IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P151

Inventor(s):

Michael Pelham and James B. Burr

Group Art Unit:

Filed:

02/03/04

Examiner:

Serial No.:

Title:

METHOD FOR GENERATING A DEEP N-WELL PATTERN FOR AN INTEGRATED CIRCUIT

DESIGN

Commissioner of Patents P. O. Box 1450 Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,489,224	METHOD FOR ENGINEERING THE THRESOLD VOLTAGE OF A	12/03/02
	DEVICE USING BURIED WELLS	
6,218,708	BACK-BIASED MOS DEVICE AND METHOD	04/17/01
6,087,892	TARGET ION/IOFF THRESHOLD TUNING CIRCUIT AND METHOD	07/11/00
6,303,444	METHOD FOR INTRODUCIING AN EQUIVALENT RC CIRCUIT IN A	10/16/01
	MOS DEVICE USING RESISTIVE WELLS	
6,048,746	METHOD FOR MAKING DIE-COMPENSATED THRESHOLD TUNING	04/11/00
	CIRCUIT	
6,091,283	SUB-THRESHOLD LEAKAGE TUNING CIRCUIT	07/18/00

Please direct all correspondence concerning the above-identified application to the following address:

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By:_

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Respectfully submitted

Reg. No. 35,295

Attorney Docket No.: TRAN-P151

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Michael Pelham and James B. Burr Group Art Unit:

Filed: 02/03/04 Examiner:

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Title: METHOD FOR GENERATING A DEEP N-WELL PATTERN FOR AN INTEGRATED CIRCUIT

DESIGN

Form 1449

U.S. Patent Documents

Examiner						Sub-	Filing
Initial	No.	Patent No.	Date	Patentee	Class	class	Date
	Α	6,489,224	12/03/02	Burr	438	526	05/31/01
	В	6,218,708	04/17/01	Burr	257	372	02/25/98
	С	6,087,892	07/11/00	Burr	327	534	06/08/98
	D	6,303,444	10/16/01	Burr	438	289	10/19/00
	E	6,048,746	04/11/00	Burr	438	17	06/08/98
	F	6,091,283	07/18/00	Murgula et al.	327	537	02/24/98

Foreign Patent or Published Foreign Patent Application

Examiner		Document	Publication	Country or		Sub-	Trans	lation
Initial	No.	No.	Date	Patent Office	Class	class	Yes	No
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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	J	
	К	
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Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.